REMARKS

It is believed that newly submitted Claims 72-75 of the present invention are novel and unobvious based on the following remarks.

The present invention is directed to a media processing apparatus having a multi-processor architecture with separate processors assigned to performing separate respective functions for efficiently decoding streams of data. New Claim 72 recites an image processing apparatus may input various kinds of data streams from an outside source representing compressed image data (e.g. data streams for digital broadcasting or DVD). The MPEG standard and the DSS standard, for example, define in the system layer different header information or the like for each kind of data stream. As a result, it is impossible for one dedicated apparatus to perform input/output processing for various kinds of data streams representing compressed image data. This problem is solved by the media processing apparatus defined in Claim 72 which is not a dedicated apparatus but a processor capable of performing input/output processing of various types and rates of data streams. With this construction, one image editing apparatus can perform the input/output processing for a plurality of kinds of compressed image data streams, only by executing a program that corresponds to the compressed image data stream to be input or output.

With regard to Claim 73, the input/output processing for the compressed image data stream is divided into a plurality of tasks. When the processor operates by single-tasking, the processor cannot switch to another task until it ends executing the current task. This prevents the processor from effectively performing the input/output processing. To the contrary, the processor defined in Claim 73 operates by multitasking. This enables the processor to perform the input/output processing effectively.

When the currently executed task is changed to another, if the instruction addresses for the currently executed task are saved into the memory and the instruction addresses for the next task are read from the memory, the start of the execution of the next task delays by the time

required for the saving and reading of instruction addresses. To prevent this, Claim 74 defines that the processor includes a plurality of program counters respectively corresponding to a plurality of tasks, and switches a currently executed task to another by instructing the instruction fetch unit to fetch instructions in accordance with instruction addresses indicated by another program counter. This enables the processor to switch, without overhead, from a currently executed task to another, that is to say, switch from a set of instruction addresses corresponding to the currently executed task to another set of instruction addresses corresponding to another task.

Claim 75 is directed to assigning a different number of instruction cycles to each task. A plurality of tasks in the input/output processing for compressed image data streams need be executed in real-time. This requires that a currently executed task switches swiftly to another task with proper timing to execute necessary processes then switches quickly to another. Some tasks require a long execution time, while others are shorter. If the same number of instruction cycles is allotted for each task, a task requiring a long execution time may be switched to another midway through execution, for example. This problem does not occur often in a personal computer with a processor having a high-speed operation clock. However, the problem often occurs in a consumer product, such as a set top box or a DVD player, into which a processor having a low-speed operation clock is incorporated. This results in a display of discontiguous image frames.

Although the discontinuous display of image frames or the real-time execution of tasks is not strictly required for personal computers, it is indispensable for consumer products. It is required for a consumer product to assure that images are played back at the same frame rate (i.e., 30 frames/second) as that on analog TVs.

According to Claim 75 of the present invention, it is possible to assign a different number of instruction cycles to each task. A task requiring a long execution time is assigned with a lot of instruction cycles so that the task is completely executed, while a task requiring a short execution time is assigned with a less number of instruction cycles so that the task does not exclusively use the processor after the task is completed. With this construction, the processor can executes a plurality of tasks in real-time. This provides advantageous effects, especially to consumer image processing apparatuses.

If the Examiner believes that a telephone interview will help further the prosecution of this case, he is respectfully requested to contact the undersigned attorney at the listed telephone number.

Very truly yours,

PRICE AND GESS

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I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to the Assistant Commissioner for Patents, Washington DC 20231
on July 31, 2002
Marc Fregoso

Signature
July 31, 2002
Date

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

New claims 73-75 were added.

Claim 72 was amended as follows:

72. (Amended) A media processing apparatus for decompressing compressed video data inputted from an outside source, comprising:

a processor for performing input/output processing affected by external factors, wherein said input/output processing includes at least inputting said compressed video data from outside and outputting decompressed video data to an external device; and

a video decoding means for decompressing said compressed video data supplied by said processor, wherein said processor processes in parallel with said video decoding means.

[an input/output processing means for performing an input/output processing of data received at a non-fixed rate; and

a decode processing means for performing decode processing of the data processed by said input/output processing means at a predetermined rate, wherein the predetermined rate at which the decode processing means processes data is independent of the non-fixed rate at which data is received by said input/output processing means.]